REMARKS

Applicant thanks the Examiner for acknowledging the claim for foreign priority and the receipt of the priority documents.

The Examiner has refused to consider the Information Disclosure Statement submitted October 11, 2000 because it does not include a concise statement of the relevance. Applicant wishes to point out that as part of the Information Disclosure Statement, Applicant provided an English language translation of portions of a Japanese Office Action in a counterpart application, which indicate the degree of relevance found by the Japanese patent office for the references cited. MPEP §609 III.A (3) provides that such a document can satisfy the requirement for a concise explanation of the relevance of the references cited. Therefore, the Examiner is respectfully requested to review and consider the references cited in the Information Disclosure Statement filed October 11, 2000, and to acknowledge same.

The Examiner objected to the Title and to several paragraphs of the Specification. The tile and relevant paragraphs of the Specification are amended. With respect to the Examiner's objection to "the delay time degradation rate calculation 305" on page 12, line 12, on the ground that it does not match Fig. 3, proposed correction of Fig. 3 is submitted herewith.

The Examiner objected to Fig. 1 on the grounds that page 2 of the specification states that delay time degradation rate calculation 105 is performed on the basis of input pin information 102 (and other information), and in Fig. 1, there is no relationship shown between 102 and 105. A proposed corrected drawing is submitted herewith.

The Examiner objected to claim 4 because of a repetition of the word "and." Claim 4 has been corrected. This change corrects a minor change in wording and is not a narrowing amendment. No estoppel is created.

The draftsperson objected to Figs. 1-6. Corrected drawings will be submitted.

Claims 1-12 are all the claims pending in the application.

Rejection of Claims 1-12 under 35 U.S.C. § 101

The Examiner rejected claims 1-12 under 35 U.S.C. § 101 on the ground that these claims are directed to non-statutory subject matter: mathematical algorithms. The Examiner stated that the claims do no recite post-mathematical operations or recite output providing a useful, concrete, and tangible result.

Applicant believes that the claims are directed to statutory subject matter under 35 U.S.C. § 101, in view of Supreme Court and Federal Circuit interpretation of the statute, including *State Street Bank & Trust Co. v. Signature Financial Group Inc*, 47 USPQ.2d 1596 (Fed. Cir. 1998).

However, to expedite prosecution, Applicant amends the claims to recite an outputting operation that outputs a useful, concrete, and tangible value. The requirements of 35 U.S.C. § 101 are met since each claim recites an algorithm applied to physical elements or process steps that outputs or fixes a useful, concrete and tangible result. (See, 47 USPQ.2d 1603). Specifically, the claims require outputting a value for use as a representative of a circuit property of a logic level circuit.

In addition, with respect to claims 7-12, each of these claims is directed to computer-readable medium.

Applicant therefore believes that all of the claims are patentable even under the Examiner's restrictive understanding of the requirements of 35 U.S.C. § 101. The Examiner stated that claims 4, 6, 10 and 12 would be allowable if the rejections under 35 U.S.C. §101 are overcome.

Rejection of Claims 1, 3, 5, 7-9 and 11 under 35 U.S.C. § 102(e)

Claims 1, 3, 5, 7-9 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Iwanishi et al., U.S. Patent No. 6,047,247. This rejection is traversed.

Applicant's claimed invention defines a unique and nonobvious method and computer product for calculating a value representative of a property of a circuit. By way of example, claims 1 and 7 require calculating the V_B from numerical values V_C, each value V_C representing a transistor property of a transistor included in the logic block. Iwanishi discloses a method of estimating hot carrier-delay degradation based on circuit information 11 and a delay library 12. The circuit information includes characteristic information of the cells, information of connection between cells and the cell-to-cell wirings such as resistance values and capacitance values. Iwanishi, col. 2, lines 59-63. The delay library contains delay parameters, such as coefficients and points of the tables used for cell delay tables, where the cell delay tables are functions with respect to input signal waveform inclinations (slew) and output load capacitance.

Iwanishi, col. 7, lines 59-65. The delay library also contains parameters necessary for calculating cell output waveforms.

Iwanishi does not disclose or suggest using for calculation V_C, a transistor property of a transistor included in the transistor block. Further, Iwanishi does not disclose or suggest using V_C for calculating V_C. Therefore, Iwanishi does not disclose or suggest all the recitations of claims 1 and 7. The Examiner points to Iwanishi col. 6, lines 37-38 and alleges that Iwanishi discloses using V_C for calculations. The passage discloses delay calculation based on circuit information 11 and a delay library 12. As discussed, the circuit information 11 and the delay library 12 do not disclose using V_C for calculation.

Further, the Examiner points to Iwanishi col. 6, lines 39-40 and alleges that Iwanishi discloses calculating V_B from using V_C. In fact, this passage discloses that the delay library 12 is used for calculating the delays of the cells and the delays of the cell-to-cell wirings. Thus, cell delay is calculated using delay parameters from the delay library such as coefficients and points of the tables used for cell delay tables, where the cell delay tables are functions with respect to input slew and output load capacitance (Iwanishi, col. 7, lines 59-65), and circuit information, which includes characteristic information of the cells, information of connection between cells and the cell-to-cell wirings such as resistance values and capacitance values. Therefore, Iwanishi does not disclose or suggest calculating V_B from V_C.

Claims 2 and 8 depend from claims 1 and 7, respectively, and therefore incorporate all of the limitation of their respective base claims. Accordingly, claims 2 and 8 are patentably

distinguishable over the prior art for at least the reasons that claims 1 and 7, respectively, are patentably distinguishable over the prior art.

In addition, claims 2 and 8 require *inter alia*, that V_C show a transistor property of a transistor connected to an input pin of the logic block. Further, claims 2 and 8 require *inter alia* that another V_C show a transistor property of a transistor connected to an output pin of the logic block. Iwanishi does not disclose or suggest using a V_C. Therefore, Iwanishi does not even remotely disclose or suggest a V_C of a transistor connected to an input pin or an output pin.

The Examiner points to Iwanishi col. 6, line 48 and alleges that the disclosed input signal waveform inclinations (input slew) calculated at delay calculation step 10 is V_C of the transistor connected to the input pin of the transistor. The Examiner cites no evidence to substantiate that the input slew is this V_C value. Further, the statement contradicts the Examiner's assertion with respect to claim 1, that V_C values are supplied by circuit information 11 and delay library 12. In point of fact, the input slew is calculated based on delay parameters relating to a cell as a whole from the circuit information 11 and the delay library 12 (see discussion above). Iwanishi does not disclose or suggest that the circuit information 11, the delay library 12, or the input slew calculated therefrom relate to a transistor property, V_C.

Similarly, the Examiner points to Iwanishi col. 6, line 50 and alleges that the disclosed output load capacitance calculated at delay calculation step 10 is V_C of the transistor connected to the output pin of the transistor. The Examiner offers no evidence for this statement and the statement is contradicted by the Examiner's earlier assertion. In point of fact, Iwanishi discloses that, like the input slew, output load capacitance is calculated based on delay parameters relating

to a cell as a whole from the circuit information 11 and the delay library 12 (see discussion above). Iwanishi does not disclose or suggest that the circuit information 11, the delay library 12, or the output load capacitance calculated therefrom relate to a transistor property, V_C.

Claims 3 and 9 require, *inter alia*, calculating the pin-to-pin delay time, based on a value, V_C, of a transistor property of a transistor included in the logic block. As discussed, Iwanishi does not disclose or suggest calculating a delay time based on V_C.

Claims 5 and 11 require, *inter alia*, calculating delay times of logic blocks according to the method of claims 3 and 9, respectively. As discussed, claims 3 and 9, respectively, require *inter alia*, calculating the pin-to-pin delay time, based on a value, V_C, of a transistor property of a transistor included in the logic block. Therefore, Iwanishi does not disclose or suggest all the recitations of claims 5 and 11. Accordingly, claims 5 and 11 are patentably distinguishable over the prior art for at least this reason.

In view of the foregoing discussion, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

for Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: August 27, 2002

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title is changed as follows:

METHOD AND COMPUTER SOFTWARE PRODUCT FOR CALCULATING AND PRESENTING A NUMERICAL VALUE REPRESENTATIVE OF A PROPERTY OF A CIRCUIT

IN THE SPECIFICATION:

The specification is changed as follows:

Page 8, fifth full paragraph

Fig. 5 shows a diagram for use in schematically describing propagation delay time ~~velocity~~ tpd when input of inverter changes from low level to high level; and

Page 10, third full paragraph

S_{out} is calculated by the next expression:

C_{out} (pF): load capacitance of transistor connected to output pin;

$$S_{out} = \alpha \left(\frac{C_{out}}{W_{out}} \right)^{\beta} \qquad (4)$$

α, β : constants depending on rounding of waveform of output pin; and

~~W_{in}~~ $\underline{W_{out}}$ (μ m): width of N-channel transistor connected to output pin.

Page 15, fourth full paragraph

In the case where AC bias has an iterative waveform at a ~~frequency~~ period T, the expression (13) is transformed into:

$$ageAC(t_{ac}) = \frac{t_{ac}}{T}\int_0^{t_{ac}} \frac{I_{ds}}{BW}\left(\frac{I_{sub}}{I_{ds}}\right)^m dt \qquad (14)$$

Page 16, fourth full paragraph

When an input signal changes from low level to high level, a transmission delay time in the inverter shown in Fig. 54 is mainly decided by N-channel transistor's ability to drive current and is shown in the following expression:

$$t_{pd} = \frac{aC}{K_n} \qquad (19)$$

a: constant; and

C: load capacitance of output.

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) A method of calculating, by the use of a computer, a numerical value V_A representative of a circuit property of a logic level circuit, from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, comprising the steps of:

(a) calculating the V_B from a plurality of numerical values V_C,~~'s~~ each value V_C ~~of which~~ representing~~s~~ a transistor property of a transistor included in the logic block; and,

(b) calculating the V_A from the V_B, and outputting V_A for use as a value representative of a circuit property of said logic level circuit.

2. (Amended) A method as in claim 1 wherein, in the step (a), each of a first group of V_C values of said plurality of numerical values V_C shows a specific ~~one of the~~ transistor property of a ~~the~~ transistor connected to an input pin of the logic block and each of second group of V_C values of said plurality of numerical values ~~another~~ V_C shows another specific ~~one of the~~ transistor property of a ~~the~~ transistor connected to an output pin of the logic block.

3. (Amended) A method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising~~the steps of~~:

(a) calculating the pin-to-pin delay time, based on a value V_C of a transistor property of a transistor included in the logic block, and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

4. (Amended) A method of calculating, by the use of a computer, pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other, comprising~~ the steps of~~:

(a) calculating an amount of stress S_{in} cast by the input pin and~~ and~~ an amount of stress S_{out} cast by the output pin according to the following expression:

when it is assumed that a load capacitance is represented by C [pF], constants

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time δ_{out} [%] according to the following expression:

when it is assumed that a constant depending on physical structure of the pin

$$\delta = \gamma\left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

is represented by γ, the term of guarantee of the LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon1$, $\varepsilon2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating <u>and outputting for use as values representative of circuit properties of said logic level circuit</u> the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

when it is assumed that pin-to-pin delay time and block-to-block delay time

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connected\_fresh}$ [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}.

5. (Amended) A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising~~ the steps of~~:

(a) calculating delay times of all said logic blocks according to the method as in claim 3; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

6. (Amended) A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising~~ the steps of~~:

(a) calculating delay times of all said logic blocks according to the method as in claim 4; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

7. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ for calculating a numerical value V_A, which shows a property of a logic level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the product making a computer execute the following processes:

(a) calculating the V_B from a plurality of numerical value V_C,~~'s~~ each V_C ~~of which~~ showing~~s~~ a property of a transistor constituting part of the logic block; and,

(b) calculating the V_A from the V_B, and outputting V_A for use as a value representative of a circuit property of said logic level circuit.

8. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ as in claim 7 wherein in process (a) one V_C shows a property of a transistor

connected to an input pin of the logic block and another V_C shows a property of a transistor connected to an output pin of the logic block.

9. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ for calculating a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the product making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit.

10. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ for calculating pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between said two logic blocks connected to each other by a computer, the product making a computer execute the following processes:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

when it is assumed that a load capacitance is represented by C [pF], constants

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

depending on change of inputted waveform are represented by α and β, and width of channel of the transistor connected to the pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time δ_{out} [%] according to the following expression:

when it is assumed that a constant depending on physical structure of the pin

$$\delta = \gamma\left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

is represented by γ, the term of a guarantee of the LSI is represented by τ [hour], constants depending on process are represented by ε1, ε2 and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

when it is assumed that pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by Tiopath_fresh [ps] and Tconnected_fresh [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by λin and λout.

11. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the product making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the product as in claim 9; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

12. (Amended) A computer-readable medium incorporating a program of instructions ~~software product~~ for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the product making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the product as in claim 10; and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).